88. The system according to claim 87, wherein said programming circuits are arranged adjacent to said memory cell array.

89. The system according to claim 80, wherein each of said programming circuits is connected to a respective one of said bit lines.

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90. The system according to claim 80, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently written.

91. The system according to claim 90, wherein said verify-termination detector is arranged on a semiconductor substrate.--

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REMARKS

The present application, at page 11, lines 27-31, incorporates by reference another application entitled "Multi-State EEprom Read and Write Circuits and Techniques", filed on the same day as the initial parent to the present application, namely April 13, 1989, by Sanjay Mehrotra and Eliyahou Harari, two of the inventors who are also named in the present application. This incorporated application is Serial No. 07/337,579, now abandoned, continuations-in-part of which have issued as patents nos. 5,163,021 and 5,172,338. The present amendment inserts a majority of the incorporated Serial No. 07/337,579 into the present application in order to support claims based thereon that are also being added by this Preliminary Amendment.

Therefore, essentially all of the Summary of the Invention, Brief Description of the Drawings and Description of the Preferred Embodiments sections of Serial No. 07/337,579 are being added to the present application. In the course of doing so, the patent numbers for referenced applications have also been added. A major revision that has been made to this added text is a change in the drawing figure numbers. Figures 1-17 of Serial No. 07/337,579 are being renumbered herein as figures 9-25, respectively, in order not to use any of the same figure numbers previously used in the present application. Tables 1 and 2 of the incorporated application have also been relabeled as figures 26 and 27, respectively. Further, the reference numbers of the drawings have been changed by adding 1000 to the reference numbers of the figures being incorporated from Serial No. 07,337,579, in order to avoid duplicating the reference numbers already used in the original figures

of the present application. Corresponding changes have been made to the text of Serial No. 07/337,579 that is being inserted into the present application.

The claims being substituted into this application are directed to programming memory cells by individually verifying when they have reached their desired programmed states. System claims 27-34, 40-42 and 44 of U.S. patent no. 5,172,338 are directed to similar subject matter with a different scope. Patent no. 5,172,338 was the subject of two reexaminations that were consolidated and which resulted in Reexamination Certificate B1 5,172,338, issued July 8, 1997.

The claims being substituted into this application are being copied from patent no. 5,657,270 of Ohuchi et al., granted August 12, 1997. Newly substituted claims 63-91 are exact copies of claims 1-17 and 43-54, respectively, of the Ohuchi et al. patent.

An Information Disclosure Statement is being filed herewith in order to provide copies of the U.S. patents discussed above and have them made of record in the present application.

A prompt examination and allowance of the present continuation application is solicited.

Dated: August 5, 1998

Respectfully submitted,

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Atty. Docket: HARI.006USS